

CLAIMS

What is claimed is:

- 1 1. A counter comprising:
2 a nonvolatile storage organized in digits having non-uniform bases; and
3 circuitry to increment a count value represented by the digits in response to
4 an increment command.
- 1 2. The counter of claim 1 wherein the nonvolatile storage includes a plurality
2 of blocks of storage cells, each of the digits being stored in a respective one
3 of the blocks.
- 1 3. The counter of claim 2 wherein one of the digits spans two or more of the
2 blocks.
- 1 4. The counter of claim 2 wherein the nonvolatile storage is a flash erasable
2 programmable read only memory in which a selected block of the plurality
3 of blocks is erased in response to an erase command that identifies the
4 selected block.
- 1 5. The counter of claim 1 wherein each of the digits includes a respective
2 number of bits according to its base.
- 1 6. The counter of claim 5 wherein the number of bits is equal to the base minus
2 one.

- 1 7. The counter of claim 5 wherein the circuitry to increment the count value
2 comprises circuitry to increment one digit of the digits by programming
3 only one bit of the one digit.
- 1 8. The counter of claim 7 wherein the circuitry to increment the one digit of
2 the digits comprises circuitry to evaluate bits of the one digit to identify a
3 least significant bit of the one digit that is in an erased state, the least
4 significant bit being the only one bit programmed to increment the one
5 digit.
- 1 9. The counter of claim 1 wherein the circuitry includes circuitry to increment
2 one of the digits and to erase each of the digits less significant than the one
3 of the digits.
- 1 10. The counter of claim 9 wherein the circuitry to erase each of the digits less
2 significant than the one of the digits comprises circuitry to concurrently
3 erase each of the digits less significant than the one of the digits.
- 1 11. The counter of claim 1 wherein the counter is a down counter and wherein
2 the circuitry to increment the count value causes the count value to be
3 reduced by one in response to the increment command.
- 1 12. The counter of claim 1 wherein the counter is monotonic, the counter
2 further comprising circuitry to prevent erasure of the digits in response to
3 detecting that a maximum count of the counter has been reached.

- 1 13. The counter of claim 1 further comprising configuration circuitry to receive
2 a counter setup command and to allocate regions of the nonvolatile storage
3 to the digits according to the counter setup command.
- 1 14. The counter of claim 13 wherein the configuration circuitry is configured to
2 store setup information specified in the setup command in a region of the
3 nonvolatile storage.
- 4 15. The counter of claim 14 wherein the region of the nonvolatile storage where
5 the setup information is stored is a one-time programmable region that
6 cannot be erased.
- 1 16. The counter of claim 14 further comprising initialization circuitry to read
2 the setup information in the region of the nonvolatile storage to identify the
3 digits of the counter.
- 1 17. The counter of claim 1 further comprising:
2 program circuitry to write data to the nonvolatile storage in response to
3 program commands received from an external source; and
4 circuitry to detect whether an address specified by one of the program
5 commands falls within a range of the nonvolatile storage allocated to
6 the digits and, if so, to disallow the program circuitry from writing
7 data at the address.
- 1 18. The counter of claim 1 further comprising circuitry to output the count
2 value represented by the digits in response to the increment command.

- 1 19. The counter of claim 1 further comprising circuitry to output the count
2 value represented by the digits in response to a read counter command.
- 1 20. The counter of claim 1 further comprising circuitry to generate a binary
2 representation of the count value for output to a host processor.
- 1 21. The counter of claim 20 wherein the circuitry to generate a binary
2 representation of the count value is configured to generate a distinct binary
3 representation of the value of each of the digits.
- 1 22. A computer system comprising:
2 a bus;
3 a processor coupled to the bus;
4 a nonvolatile memory device coupled to the bus to receive commands from
5 the processor, the commands including an increment command, the
6 nonvolatile memory device including
7 a nonvolatile storage array organized in digits having non-uniform
8 bases; and
9 circuitry to increment a count value represented by the digits in
10 response to the increment command.
- 1 23. A computer system comprising:
2 a bus;
3 a processor coupled to the bus;
4 a security co-processor coupled to the bus to receive commands and data
5 from the processor; and

6 a nonvolatile memory device coupled to receive commands from the
7 security co-processor, the commands including an increment
8 command, the nonvolatile memory device including
9 a nonvolatile storage array organized in digits having non-uniform
10 bases; and
11 circuitry to increment a count value represented by the digits in
12 response to the increment command.

1 24. A method comprising:

2 receiving a command to increment a counter implemented in a nonvolatile
3 storage device, the nonvolatile storage device including a nonvolatile
4 storage array organized in digits that have non-uniform bases, the
5 digits defining the counter;
6 searching each of the digits in order of significance until a least significant
7 unprogrammed bit of one of the digits is found; and
8 programming the unprogrammed bit to carry out the increment command.

1 25. The method of claim 24 further comprising erasing bits of each of the digits
2 less significant than the one of the digits containing the unprogrammed bit
3 to carry out the increment command.

1 26. The method of claim 24 further comprising receiving a command specifying
2 a base for each of the digits of the counter.

1 27. The method of claim 24 further comprising receiving a command specifying
2 a quantity of the digits.
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